Large area Gamma-ray Imaging Detector Based on High Resolution CdTe Diode

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Abstract—
We are developing a large array detector composed of 1024 individual CdTe diodes. Each detector has the dimensions of 1.2 mm × 5.0 mm and a thickness of 1.2 mm. An edge-on geometry is used for the injection of γ-rays, to obtain a cross-section thickness of 5 mm. With this geometry, the distance between the two electrodes can be kept small, and we can therefore apply the high electric field which is necessary to achieve a high energy resolution (by reducing the low energy tail) and also to sustain the long-term stability of the CdTe diode. Signals from each detector element are fed into newly developed low noise ASICs. We use 32 chips for the readout of 1024 elements. In this paper, we report the basic characteristics of the individual detectors and the overall performance of the gamma-camera. Design of the readout electronics system is also described.

Index Terms— **CdTe, gamma-ray, gamma camera.**

I. Introduction

THE high absorption of cadmium telluride (CdTe) and cadmium zinc telluride (CdZnTe), comparable with that of NaI(Tl) and CsI(Tl), is a very attractive features for the next generation of gamma-ray detectors (see review [1], and references therein). Imaging detectors for γ-rays, especially for energies around several hundred keV, are a major goal in various fields including astronomical and medical applications.

In fact, there are increasing demands to have CdTe and/or CdZnTe detectors with sizes larger than 20 cm^2 for imaging with spatial resolution better than 1-2 mm. For astrophysical applications, the detector will be used as a part of new generation Compton telescope and a detector plane for a coded-mask imager. For these applications, in particular for the use as the absorber in the Compton telescope, high energy resolution is the key factor to improve not only the sensitivity to detect γ-ray lines from celestial objects but also the angular resolution. In order to operate the detector with an active shield made of scintillator, a timing resolution as fast as a few microseconds would be required. The integration of readout electronics to handle several hundred to several thousand channels is also a crucial issue.

We are now developing a large array detector composed of 1024 individual CdTe diodes for balloon-borne experiments. In this paper, we report the basic characteristics of individual detector elements and the overall performance of the first prototype detector. Design of the readout electronics system utilizing a newly developed low noise ASIC is also described.

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II. Schottky CdTe Diode under Edge-on Geometry

The uniform charge transport properties of wafers are a very important aspect not only for fabricating large area strip or pixel detectors but also for constructing a large scale gamma-ray camera consisting of many individual detectors. The CdTe crystal used here is based on single crystal grown by the Traveling Heater Method by ACRORAD (THM-CdTe) [2]. We found that the uniformity of the CdTe wafer produced by this method is very high when we constructed large area CdTe diode detectors [3], [4]. Therefore, when we construct a detector with many elements, the yield of selecting detectors with almost uniform characteristics, such as mobility-lifetime products, is very high.

Energy resolution is one of the most important characteristics of semiconductor detectors. We have reported a significant improvement in the spectral properties of CdTe detectors by means of a Schottky diode (CdTe diode) [3], [5], [6]. The very low leakage current of the CdTe diode enables us to apply a high electric field to ensure complete charge collection in relatively thin devices. The improvement of the energy resolution by adopting the Schottky junction is drastic. However, once the diode is formed, the detector shows the degradation of gain and resolution with time (*polarization*) under certain operating conditions, which is not seen in THM-CdTe based detector with ohmic contacts for anode and cathode. We have found that both a high electric field of several kV cm^{-1} and a low operating temperature (below several degrees Celsius) ensure

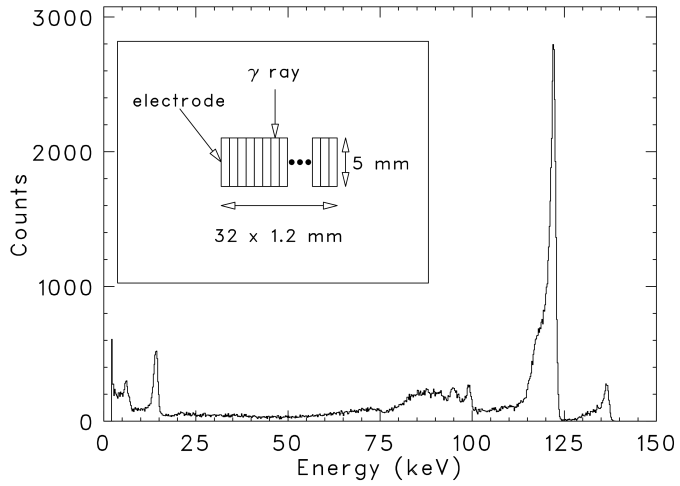

Fig. 1. Energy spectrum of ^{57}Co obtained with a single element of the 1024-array detector. The applied bias voltage is 1000 V and the operating temperature is −20 °C . The detector has dimensions of 1.2 mm × 5.0 mm and a thickness of 1.2 mm. As shown in the insert, an edge-on geometry is used for each detector to improve the detection efficiency by keeping the good energy resolution of the CdTe diode. Thirty-two rows of 32 individual detectors are combined into one large detector.

stability on time scales longer than days.

In order for CdTe and CdZnTe to have a sufficient detection efficiency for the 511 keV line from electron-positron annihilation, which is one of the important targets in high energy astronomy, the detector should be at least 5 mm thick. This efficiency, however, assumes that we can collect all electron-hole pairs generated in the detector. If we use a face-on geometry, where γ-rays irradiate from the cathode face, the reduction of the pulse height is severe for events which take place close to the anode electrode due to the poor charge transport properties, especially for holes in CdTe and CdZnTe; the actual efficiency becomes very poor for γ-rays with energies above several hundred keV [1].

In the 1024-array CdTe detector, we adopted an edge-on geometry for the injection of γ-rays (Fig. 1). This geometry has an advantage over the face-on geometry, because the distance between the two electrodes can be kept small, and we can apply the high electric field which is necessary to achieve the high energy resolution by reducing the low energy tail.

III. Large Area Gamma-ray Camera

Fig. 2 shows a photo of a prototype CdTe imaging detector. The detector has 32 rows, each consisting of 32 individual elements. The total area covered by the detector is 44.6 mm × 44.6 mm (including 0.2 mm gaps between each element). The intrinsic spatial resolution of 1.2 mm is given by the cross-section of the individual detector element. In comparison with monolithic type detector with pixellated electrodes, uncertainty of the position due to the

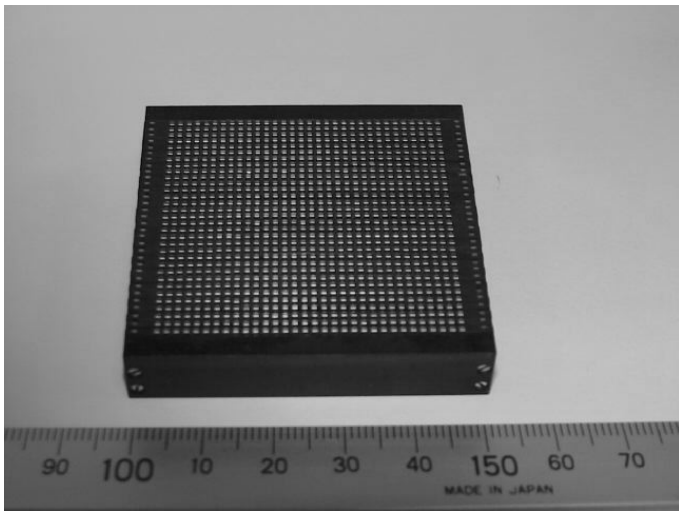

Fig. 2. A picture of the first prototype large 1024-array detector based on the high resolution CdTe diode. The pads from electrodes for the 1024 individual elements are shown. The total area covered by the detector is 44.6 × 44.6 mm^2, including the gaps between detector elements.

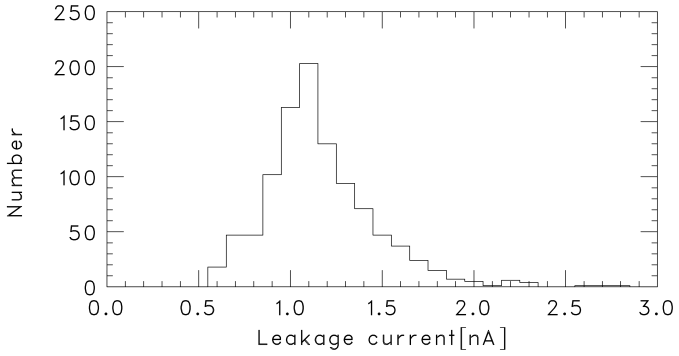

Fig. 3. Distribution of the leakage current measured from 1024 CdTe diode elements under the bias voltage of 700 V at 25 °C .

charge sharing among the adjacent pixels does not occur. An energy resolution of ∼ 1.4 keV was achieved for each detector element using a conventional preamplifier (CP5109 by Clear Pulse) for operation at −20 °C .

Distribution of the leakage current measured from the prototype detector is shown in Fig. 3. The average leakage current of 1024 elements is 1.2 nA for operation at 25 °C under the bias voltage of 700 V. When the detector is cooled to −20 °C , the leakage current goes down to 100 pA at 700 V and 50 pA at 500V.

After the prototype detector was assembled, we checked how many of the 1024 channels could be read out. By measuring individual pixel, we found that the first array has an yield of 85%. By tuning the connection mechanism, we found that this value can be increased up to 95% in the succeeding arrays.

IV. Readout Electronics

For astrophysical applications, the readout system should be very compact, because size and weight are very limited in balloon-borne or satellite-borne experiments. We

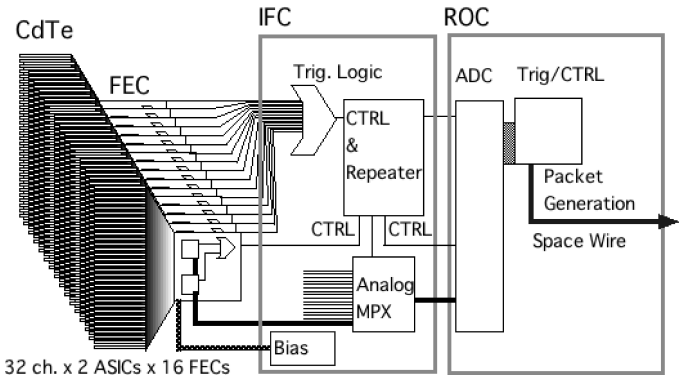

Fig. 4. Schematic Diagram of the Readout system.

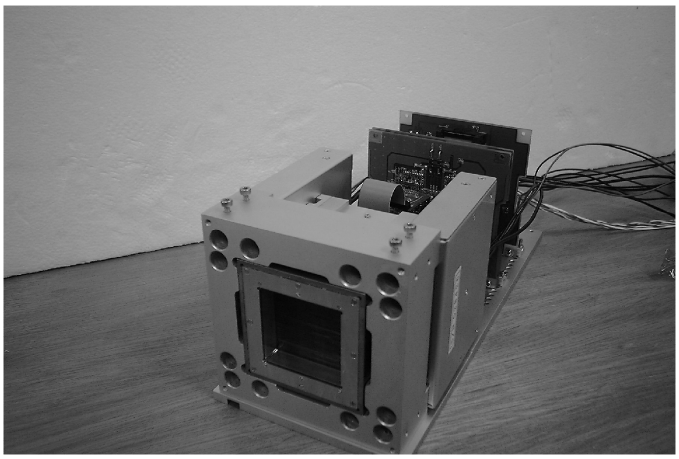

Fig. 5. A picture of the first prototype 1024-array CdTe detector and the readout.

designed a new read-out electronic system from the front-end ASICs to the downstream digital processing electronics. The schematic diagram of the readout electronics is shown in Fig. 4. Signals from each CdTe detector are read out by the VA32TA front-end ASIC via a pitch adapter. The VA32TA is a 32-channel, low noise CMOS ASIC which includes, on a per-channel basis, a preamplifier, shaper, sample/hold, analog multiplexer and discriminator. Two VA32TAs are mounted on the FR4 front-end cards (FEC). Sixteen FECs are connected to an interface card (IFC) by 0.635 mm pitch flat ribbon cables. The readout-card (ROC) performs analog-to-digital conversion and readout sequence control. A packet of data is constructed on an event by event basis in the ROC and sent to an interface board in the data acquisition computer via IEEE 1355 Space Wire network. The IFC provides analog bias currents/voltages, and digital and analog signal repeater functions. Fig. 5 is the photo of the newly developed 1024-array CdTe detector and the readout system. The whole system has dimensions of 10 cm $\times$ 10 cm and depth of 30 cm. CdTe detectors are mounted in the center of the front panel.

A. Low noise analog ASIC "VA32TA"

We have developed the VA32TA front-end ASIC based on the VA32C amplifier VLSI and the TA32C trigger VLSI originally developed by Ideas. A detailed description of Viking-architecture chip is given elsewhere [7], [8]. The VA32TA is fabricated in the AMS 0.35 μm technology, which is measured to be radiation tolerant to 20 MRad or more [9]. One chip of the VA32TA contains 32 channels of signal-readout. Each channel includes a charge sensitive preamplifier-slow CR-RC shaper-sample/hold-analog multiplexer chain (VA section) and fast shaper-discriminator chain (TA section) as illustrated in the block diagram of Fig. 6. It consumes 4.5 mW/channel in the VA section and 1.8 mW/channel in the TA section.

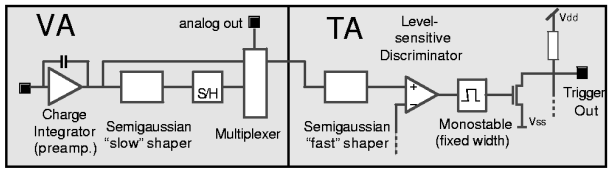

Fig. 6. Block diagram of VA32TA front-end LSI.

The front-end MOSFET size for the preamplifier is optimized for small capacitance load, to attain optimal noise performance. The preamplifier is followed by $CR-RC$ shaper to optimize the noise performance by controlling the peaking time. The expected noise performance is $(45+19\times C_d)/\sqrt{\tau}$ e^- (RMS) in ENC or $(0.37+0.16\times C_d)/\sqrt{\tau}$ keV (FWHM), where C_d is the load capacitance and τ is the peaking time, which can be varied from 1 to 4 μs. The output of the shaper is fed to a track and hold, which consists of a capacitor and a CMOS switch. The voltages on the capacitors are connected through high-input-impedance buffers and a second set of CMOS switches to an output amplifier. A single bit propagating through a shift register causes these output switches to be closed one at a time. In this way all 32 channels in the chip can be read using a single ADC.

The peaking time of the fast shaper in the TA section can be either 75 ns or 300 ns. A trigger signal is produced by a wired-OR of discriminator outputs from all channels and driven by an open drain output circuits to facilitate wired-OR of trigger signals from multiple chips.

Feedback resistors for the preamplifier, as well as slow and fast shapers, are realized with MOSFETs. Gate voltages of the feedback MOSFETs are controlled by internal DACs (digital-to-analog converters) on the chip. Bias currents for various components are also controlled by the internal DACs. Threshold levels can be adjusted for each channel using individual 4-bit DACs to minimize threshold dispersion. A 200-bit register is required to hold the values for all internal DACs. Majority selector logic circuitry has been utilized for these registers to ensure the tolerance against single-event upsets (SEUs), which is important for space applications. This majority selector circuitry uses three flip-flops for each bit and takes a majority of the three

when they become inconsistent. This logic also generates a signal when such inconsistencies are detected.

B. Front-end Card

A small number of passive surface mount components are added to the FEC for bypassing, calibration, and clock termination. Double-row 1.27 mm pitch connectors were selected to meet space requirements from the mechanical support. The substrate is made of FR4 for production flexibility. Special care is taken to optimize the heat conductivity from the ASICs as the FECs are packed into small volume in high density. Thirty five thermal via are placed underneath the ASICs to maximize the heat path to the heat spreader attached to the bottom of the FEC.

C. Interface Card and Readout Card

Trigger signals from each FEC are ORed in the IFC. Once the trigger signal is received from one of the FECs, the IFC disables further trigger signals in the FEC, then sends a trigger signal to the ROC. The ROC module controls the readout sequence and transfers the data to the data acquisition system. When an ROC receives the trigger signal from IFC, it sends sample-and-hold signal to all FECs through IFC. In order to minimize the dead time for converting analog signals from the detector, the ROC reads analog signals only from the FEC which produces the trigger. The information of the adjacent channels, which are read out with the triggered channel in the FEC, is important to subtract common-mode noise. In the ROC, a high performance complex programmable logic device (CPLD) and flash ADC (FADC) are mounted on a 10 cm $\times$ 10 cm board. We use EP20K100ETC144-2x manufactured by Altera Corporation. It has 4,160 logic elements and 52 $\times$ 1024 memory bits, which are equivalent to 262,912 system gates. The logic of the CPLD is designed by VHDL hardware definition language, and loaded through the boundary scan chain, "JTAG" (IEEE 1149.1). It can also be stored in the on-board EEPROM. The system clock of the logic is provided by an onboard 48MHz clock module. A part of logic works at a higher clock rate, which is provided by on-chip PLL circuit. As for the control and data transfer link to data acquisition system, the serial data transfer protocol IEEE 1355 Space Wire standard was chosen. Space Wire uses low voltage differential signaling (LVDS). Its data rate is comprised between 2 Mbps and 100 Mbps. Much higher speed is possible if we use multiple lines with a router configuration. For the present system, we implement the protocol at 24 Mbps for ROC. Logic blocks on the chip are controlled and monitored through the Space Wire data link.

V. Performance

To characterize the basic performance of VA32TA combined with the CdTe detector, we obtained a ^{57}Co spectrum using a single mounted CdTe test piece, which has the same dimensions with the one mounted in the 1024-array detector. Signals from the detector were processed via the VA32TA chip, controlled by commercial LSI test system ("VADAQ") provided by Ideas. The time constants in the VA32TA chip were set to 3 μs for the slow shaping(VA) and 0.3 μs for the fast shaping(TA). The operating temperature was -20 °C under the bias voltage of 500 V. The resultant spectrum is shown in Fig. 8(a). The energy resolution of 122 keV line is measured to be about 5 keV (FWHM). Further analysis of the noise performance of VA32TA chip and the results obtained with a double-sided silicon strip detector are described in our separate publication [10].

Next, we combined the array detector with the readout system. The total power of the system is measured to be 10 W. Currently, half of the detector array are noisy, possibly due to the electric mismatch on the connection mechanism. Thus, we disabled the triggers of corresponding channels of VA32TAs and concentrated on another half of the array. To obtain an image with the system we have developed, we placed two M8 nuts in front of the array detector and irradiated with a ^{57}Co source, which is placed 10 cm apart from the detector. It is a point source with an activity of about 3 Mbq. Fig. 7 is the image of the nuts, zoomed to a half of the whole detector. Fig. 8(b) presents the spectrum from one of the best channels. The energy resolution is about 5 keV(FWHM) at 122 keV. By comparing Fig. 8(a) and (b), it is shown that our 1024 channel system can properly handle numbers of VA32TA LSIs, in spite of its high density and complexity. Thirty-seven of 512 channels do not work properly due to misconnection of spring pins used for the connection between the CdTe and LSI.

VI. Conclusion

The high energy resolution of the CdTe diode is very attractive for hard X-ray and gamma-ray detection. Many concepts based on the high resolution CdTe diodes are now being investigated and the prototype detectors are being developed [3]. Especially, the CdTe array detector with an area of several 10 cm^2 and position resolution of $\sim$mm is the key device for gamma-ray observations, which we plan to perform by using scientific balloons. It is also useful in various fields including medical applications [11]. We have fabricated the prototype of such a detector, based on high energy resolution CdTe diode and newly developed ASICs. A space Wire based compact data acquisition system to handle 1024 read-out channels from 32 ASICs is also developed for this purpose.

References

[1] T. Takahashi and S. Watanabe, "Recent progress on CdTe and CdZnTe detectors," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 950-959, 2001.

[2] M. Funaki, T. Ozaki, K. Satoh, and R. Ohno, "Growth and characterization of CdTe single crystal for radiation detectors," *Nucl. Instrum. Methods*, vol. A 436, pp. 120-126, 1999.

[3] T.Takahashi, T. Mitani, Y. Kobayashi, M. Kouda, G. Sato, S. Watanabe, K. Nakazawa, Y. Okada, M. Funaki, R. Ohno, and K. Mori, "High-resolution Schottky CdTe diode detector", *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 1297-1303, 2002.

[4] K. Nakazawa, T. Takahashi, S. Watanabe, G. Sato, M. Kouda, Y. Okada, T. Mitani, Y. Kobayashi, Y. Kuroda, M. Onishi, R. Ohno, H. Kitajima, "Large area CdTe diode detector for space application," *Nucl. Instrum. Methods*, to be published.

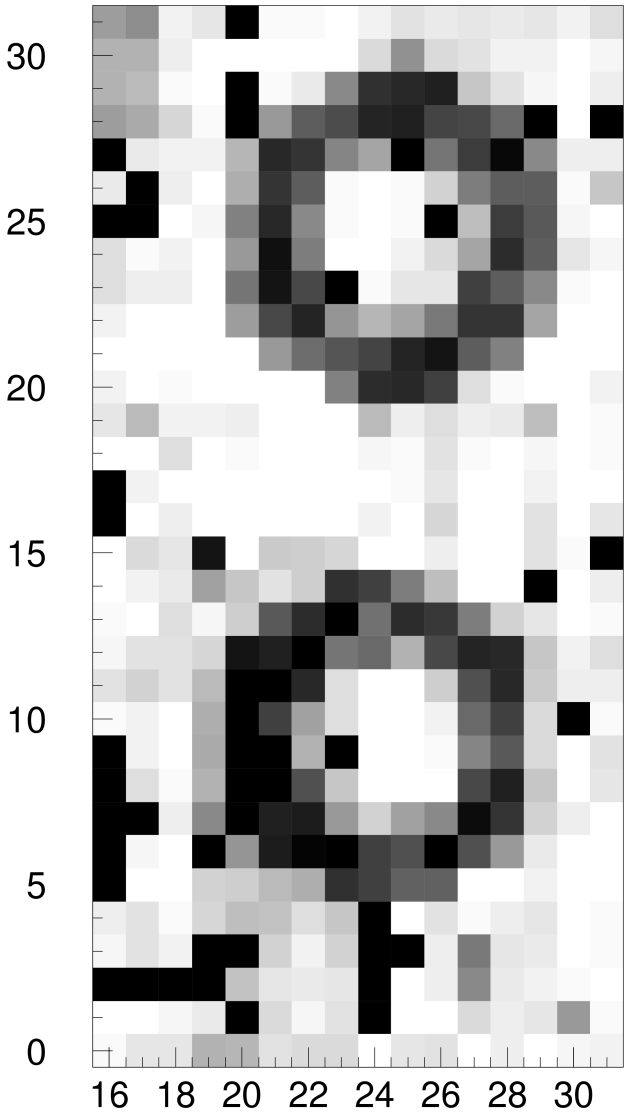

Fig. 7. A ^{57}Co gamma-ray image of two M8 nuts taken with a half part (about 22 mm × 44 mm) of the detector, via the newly developed readout system. The system was operated at −20 °C and the bias voltage was 200 V. Events included in the 122 keV peak were selected to produce the image. Thirty-seven of 512 channels do not work properly due to misconnection of spring pins used for the connection between the CdTe and LSI.

[5] C. Matsumoto, T. Takahashi, K. Takizawa, R. Ohno, T. Ozaki, and K. Mori, "Performance of a new Schottky CdTe detector for hard x-ray spectroscopy," *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 428-432, 1998.

[6] T. Takahashi, K. Hirose, C. Matsumoto, K. Takizawa, R. Ohno, T. Ozaki, K. Mori, and Y. Tomita, "Performance of a new Schottky CdTe detector for hard x-ray spectroscopy," in *Proc. SPIE* vol. 3446, 1998, pp. 29-37.

[7] E. Nygård, P. Aspell, P. Jarron, P. Weilhammer, and K. Yoshioka, "CMOS low noise amplifier for microstrip readout design and results," *Nucl. Instrum. Methods*, vol. A 301, pp. 506-516, 1991.

[8] O. Toker, S. Masciocchi, E. Nygård, A. Rudge, and P. Weilhammer, "VIKING, a CMOS low noise monolithic 128 channel frontend for Si-strip detector readout," *Nucl. Instrum. Methods*, vol. A 340, pp. 572-579, 1994.

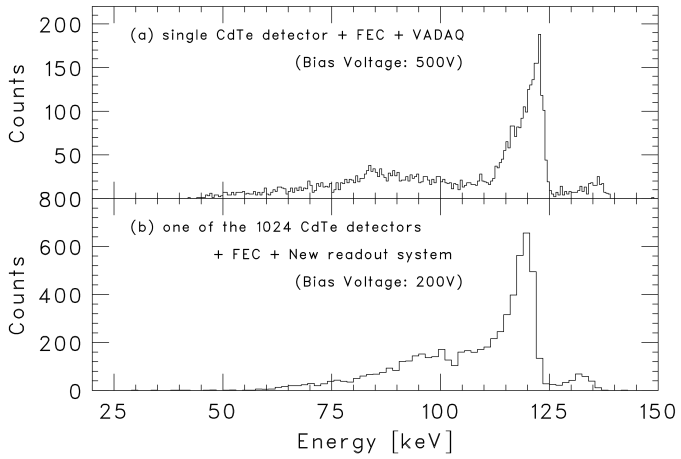

Fig. 8. (a) Energy spectra of ^{57}Co obtained from a single CdTe detector, connected to VA32TA operated with VADAQ(Ideas). (b) The same from a certain channel of the 1024-array detector, operated with the new readout system. In both cases, the operating temperature was −20 °C .

[9] M. Yokoyama, H.Aihara, M.Hazumi, H.Ishino, J.Kaneko, Y.Li, D.Marlow, S.Mikkelsen, E. Nygård, H.Tajima, J.Talebi, G.Varner, and H.Yamamoto, "Radiation hardness of VA1 with sub-micron process technology," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 440-443, 2001.

[10] H. Tajima, T. Kamae, S. Uno, T. Nakamoto, Y. Fukazawa, T. Mitani, T. Takahashi, K. Nakazawa, Y. Okada, and M. Nomachi, "Low noise double-sided silicon strip detector for multiple-Compton gamma-ray telescope", in *Proc. SPIE*, to be published.

[11] M. Tsuchimochi, H. Sakahara, K. Hayama, M. Funaki, T. Shirahata, T. Orskaug, G. Maehlum, K. Yoshioka, E. Nygård, "Performance of a small CdTe gamma camera for radio-guided surgery", in *Proc. SPIE*, vol. 4508, 2001, pp. 74-87.