

Single Photon Counting X-ray Imaging with Si and CdTe Single Chip Pixel Detectors and Multichip Pixel Modules

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Abstract—Multichip modules (MCM) have been successfully built and operated. These use 4 single-photon counting MPEC 2.3 chips that are bump bonded to 1.3 cm x 1.3 cm CdTe or Si semiconductor pixel sensors. Single-chip detectors were built as well.

The MPEC 2.3 chip provides a pixel count rate up to 1 MHz with a large dynamic range of 18 bits, 2 counters and energy windowing with continuously adjustable thresholds. Each MPEC has 32 x 32 pixels of 200 μm x 200 μm pixel size. For a MCM the 4 chips are arranged in a 2 x 2 array which leads to a 64 x 64 sensor pixel geometry. The MCM construction is described, and the imaging performance of the different detectors is shown. A newly developed USB readout system has been used.

I. INTRODUCTION

Single photon counting with hybrid pixel detectors has been introduced as a suitable method for direct digital imaging [1], [2]. Advantageous for a hybrid pixel detector is the use of different semiconductors as sensor material. As Si is a well understood semiconductor and homogeneous large Si wafers are easily available, Si is the preferred sensor material for applications where a high flux of ionizing radiation is used, e.g., material science or protein crystallography [3]-[8].

On the other hand, the low atomic number of Si ($Z=14$) leads to a low absorption efficiency for X-rays with energies higher than a few 10s of keV. This is not acceptable in low-dose medical imaging applications or hard X-ray and γ -ray astronomy. Thus, high Z -materials like GaAs ($Z=31/33$) were studied [9]-[11]. In addition, a very promising material for high

absorption sensors is CdTe ($Z=48/52$). The absorption efficiency of a 0.5 mm thick CdTe sensor is 90 % and 30 % for X-ray energies of 40 keV and 100 keV, respectively. In addition, progress in wafer production and electrode design allows high quality sensors with excellent spectroscopic performance [12]-[19]. As a thin CdTe sensor is very sensitive to shear forces and the electrode metalization can not be exposed to high temperatures, it is difficult to obtain a reliable connection of the readout chip to the CdTe sensor. Therefore, a sophisticated gold stud bump bond process was developed at ISAS (Institute of space and astronomical science, Japan) and a 0.5 mm thick CdTe sensor was successfully bonded and operated with a previous version of the MPEC chip [20].

In order to use single photon counting detector systems for imaging applications, it is necessary to cover a large imaging plane, which is achieved with multichip modules (MCM). This means that several readout chips are bump bonded to a single large sensor. In this work an arrangement of a square geometry with 2 x 2 MPEC chips was chosen and systems with Si or CdTe sensors, each covering an active detection area of about 13 mm x 13 mm, were successfully built and operated.

In this paper we present the MPEC 2.3 chip and report on studies with Si sensor MCMs and, for the first time, on measurements with single photon counting CdTe sensor MCMs.

II. PIXEL DETECTOR DESCRIPTION

A. Readout chip

The MPEC 2.3 chip is a single photon counting pixel chip with 1 MHz count rate capability and energy windowing for photon energy discrimination. The active area of 6.4 mm x 6.4 mm is structured into 32 x 32 pixels of 200 μm x 200 μm size. Every pixel cell contains a preamplifier, two independent discriminators, and two 18 bit counters (Fig. 1). A coarse discriminator threshold is set globally, and a fine adjustment can be applied dynamically for both discriminators in each pixel. This dynamic adjustment is performed by storing a correction voltage on a capacitor. The independent discriminators allow an energy window to be set, which can be

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useful in medical imaging for contrast enhancement [21]. The MPEC 2.3 chip is based on the MPEC 2.1 chip [22], and some crucial parts of the chip layout were reworked (counter, shift register, multiplexer, implementation of a new window-logic). The design of the MPEC 2.3 was done in the AMS 0.8 μ m technology. Unfortunately, this process offers only two metal layers which makes an efficient shielding between the digital part and the analog part of the chip difficult.

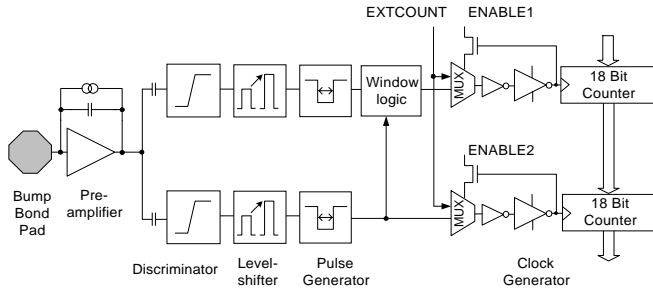


Fig. 1. Schematic of one pixel of the MPEC 2.3 chip.

B. Sensors

For the presented measurements, single chip sensors as well as MCM sensors were used. The 280 μ m thick Si sensors are high resistance p+ on n sensors operated in diode configuration and the connection to the MPEC 2.3 chips is achieved by a wafer-level solder bump bond process at IZM (Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, Berlin, Germany) [23]. The p+ electrode is structured into the corresponding number of pixels of the readout chip, and the pixel matrix is surrounded by a guard ring of 200 μ m width.

The 0.5 mm thick high resistance CdTe sensors were fabricated by ACORAD [24], and the detector assembly was done by ISAS. Both sides of the ohmic detectors are plated with Pt electrodes, and the side connected to the readout chip is structured into the corresponding number of pixels. Again, the pixel matrix is surrounded by a guard ring of 200 μ m width. For the chip sensor connection a special gold stud bump bond technique in combination with an epoxy resin was used. More details of this sophisticated bonding procedure and characteristics of the used CdTe can be found in [20].

A critical issue for building MCMs is the handling of the spacing between the readout chips (inter-chip region). The readout chips have to be designed in a way that they are buttable at least at three sides, i.e., wire bond pads should only be placed on one chip side. Also, the sensor pixels which are connected to the corresponding pixels at the buttable edges of the readout chips have to be larger than the normal pixel size because some additional space between the readout chips is required. Therefore, these pixels have a double side length in one direction leading to an area twice as large as the area of a normal pixel ("double pixel"). The four pixels in the center of the sensor have the double side length in both directions, thus,

having a four times larger area ("quad pixel"). The arrangement of double and quad pixels can be seen schematically in Fig. 2. For the Si sensor a double pixel has a size of 200 μ m x 400 μ m (quad pixel: 400 μ m x 400 μ m) whereas for the CdTe sensor a double pixel geometry of 200 μ m x 450 μ m was chosen (quad pixel: 450 μ m x 450 μ m). Algebraically, the gap between the readout chips should be 400 μ m (450 μ m for the CdTe module), but as the readout chip has a surrounding margin, the effective gap between adjacent readout chips is only about 200 μ m, making MCM bump bonding challenging.

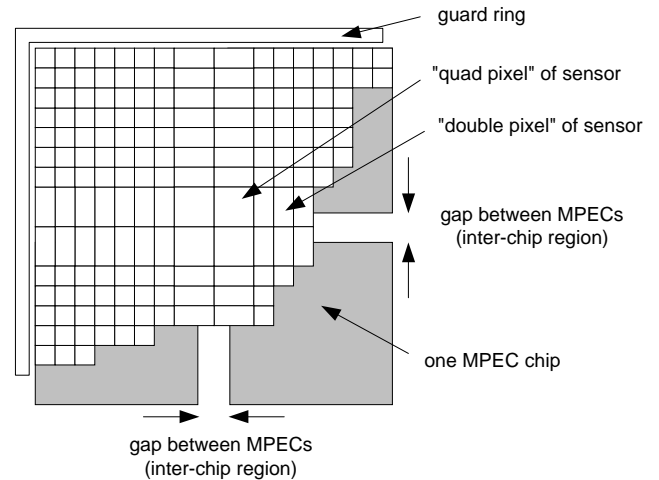


Fig. 2. Schematic view of a MCM with large pixels in the inter-chip region.

C. Readout system

All measurements with single chip detectors and with MCMs were done with a newly developed USB-based data acquisition system (Fig. 3).

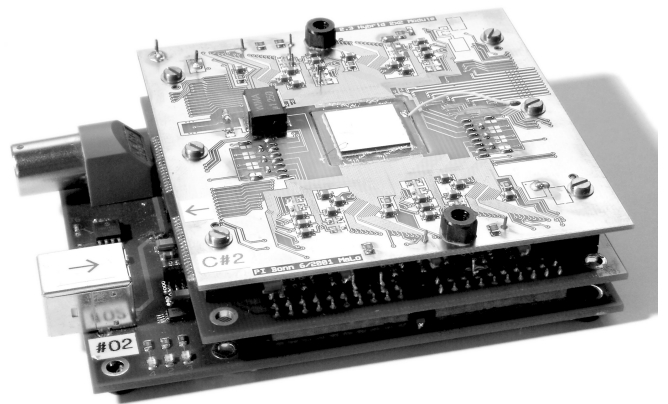


Fig. 3. Photograph of the USB-based detector system with a 2 x 2 CdTe sensor MCM (center of top PCB).

This small and handy system is controlled by only a laptop computer and is easily transported and set up. The system can

be powered by the USB-line and, with a battery stack for the detector depletion voltage, the whole system is independent of an external power supply. Fig. 4 shows the compact stack arrangement of 3 PCBs. The USB device controller card which is performing the communication between the detector and the PC is placed in the bottom of the stack. Above it is the analog support card, which contains the analog and digital circuits necessary for detector operation. On top, the detector hybrid board is mounted by a zero force connector.

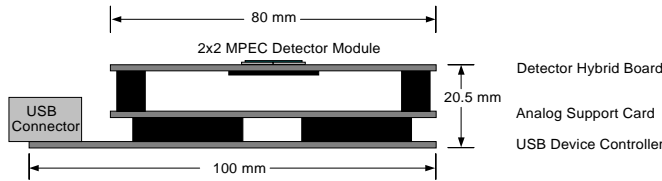


Fig. 4. Schematic view of the USB readout system for MCMs and single chip detectors. A stack of three PCBs makes the system compact and mobile.

In order to avoid mechanical stress due to shear forces originating from the mismatch of thermal expansion coefficients or external forces, the detector module itself is not fixed to the detector hybrid board but to a small metalized ceramic plate. This ceramic plate in turn is put through a corresponding opening in the detector hybrid board and fixed with another ceramic plate (Fig. 5). The use of ceramic material ensures a good match of the thermal expansion coefficient of Si and a good heat transfer during chip operation.

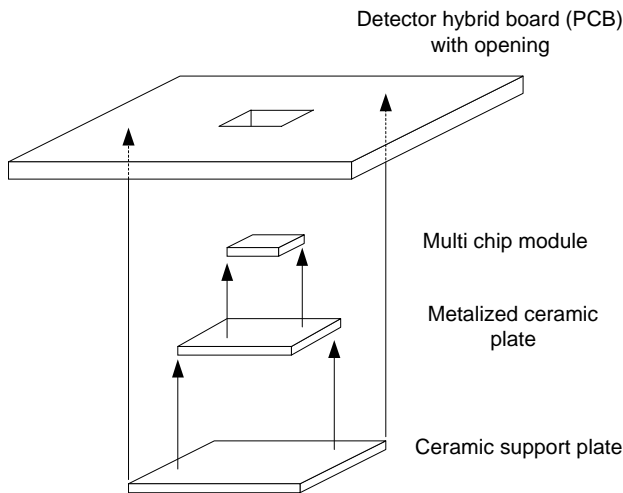


Fig. 5. Assembling of the ceramic plates connecting the MCM to the detector hybrid board.

III. MEASUREMENTS WITH SINGLE CHIP DETECTORS

A. Thresholds

The MPEC 2.3 is a low noise ASIC designed for hole collection in Si sensors. The equivalent noise charge (ENC) is measured to be typically $60 \pm 12 e^-$ without sensor. With the additional input capacitance due to the sensor the noise for a $500 \mu\text{m}$ thick CdTe sensor is $80 \pm 20 e^-$ and for a $280 \mu\text{m}$ thick Si sensor $105 \pm 20 e^-$. The threshold dispersion is about $180 e^-$ for a MPEC without sensor or a Si sensor whereas for a CdTe sensor the threshold dispersion is about $300 e^-$. This increase in threshold dispersion is not completely understood and might be related to the used gold stud bump bond process. All noise and threshold dispersion values vary only a little for chips with the same sensor material.

Also, it is possible to collect electrons with the MPEC chip. This electron collection mode has less performance than the hole collection mode (e.g. limited linearity, no threshold fine adjustment available yet). Since the operation of a CdTe sensor requires electron collection, all measurements with a CdTe sensor are done in the electron collection mode. The minimum threshold that can be set for a Si sensor in hole collection mode is about $1300 e^-$, and for a CdTe sensor in electron collection mode the minimum threshold is some $100 e^-$ higher. The high threshold has to be set to avoid digital-to-analog cross talk and is not in contradiction to the low noise performance of the chip. The digital switching noise couples into the preamplifier via the chip bulk and the sensor. If the threshold were not high enough, the digital switching noise would cause false signals. As mentioned earlier, effective shielding could not be achieved in the AMS $0.8\mu\text{m}$ technology in which only two metal layers are available.

An important characteristic for the imaging performance of a photon counting chip is a low dispersion of the thresholds of all pixels in order to set low thresholds and fine energy windows by the double threshold feature. In the case of the MPEC 2.3 chip, both thresholds of a single pixel can be independently adjusted by storing a correction voltage on a capacitor in each pixel. As a result, the RMS-value of the threshold dispersion without a sensor could be reduced from $180 e^-$ for the unadjusted case to $10 e^-$ for the adjusted case (Fig. 6 and 7). In previous work, a low threshold dispersion was demonstrated with the MPEC 2.1 [22]. However, the outer columns of the MPEC 2.1 chip did not work properly, whereas this problem is eliminated in the MPEC 2.3.

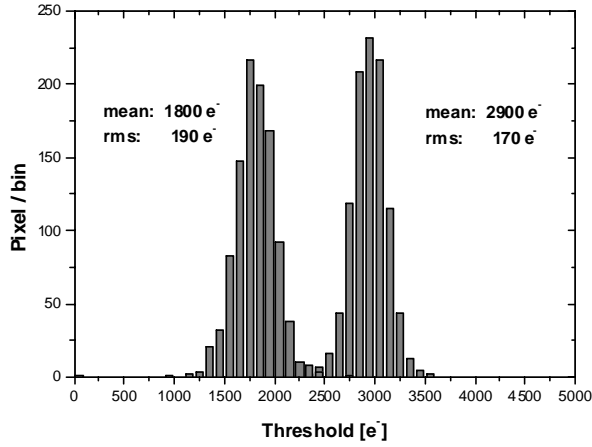


Fig. 6. Dispersion of unadjusted lower and upper thresholds of MPEC2.3 (without sensor).

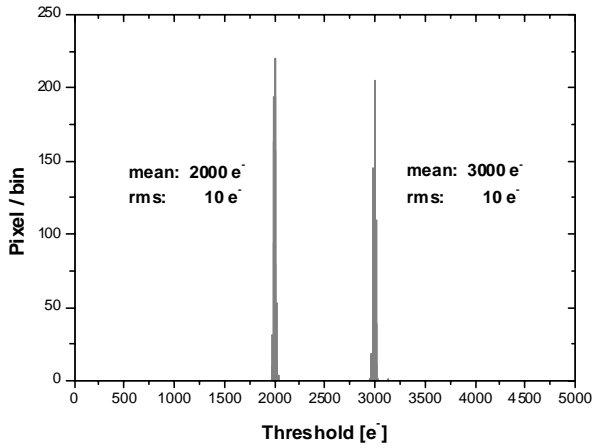


Fig. 7. Dispersion of adjusted lower and upper thresholds of MPEC2.3 (without sensor).

As the threshold adjustment is done dynamically, the correction voltage needs to be refreshed. In order to minimize the refresh rate, a threshold drift compensation circuit was developed to reduce the drift current from the capacitor [22]. As an example, the measured drift of the lower threshold of the 32 pixels of one column is shown in Fig. 8. At the beginning of the measurement the thresholds were set to $3000 \pm 10 e^-$, and then they were measured every 2 minutes. It turns out that the maximum drift rate is $< 0.2 e^-/s$. With the existing readout system it takes about 1 min to fine adjust serially all 2048 discriminators of a chip, but a hardware implementation of the adjustment procedure (e.g. use of a field programmable gate array) would reduce the adjustment time to about 100 ms.

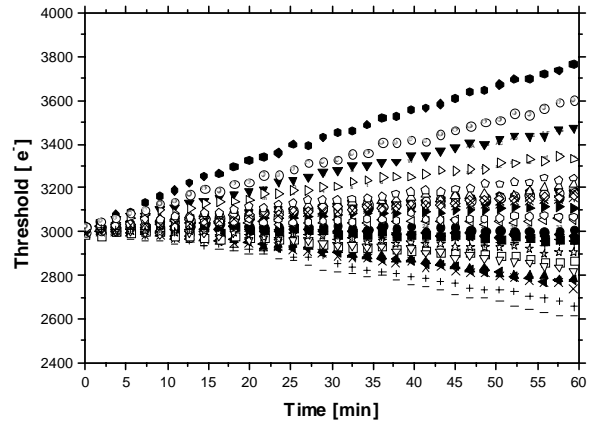


Fig. 8. Threshold drift of 32 pixels within one hour.

B. Imaging

As described earlier, the threshold settings were limited by digital-to-analog cross talk. This resulted from the counter flip-flops of a pixel cell and the switching noise of digital control lines. The influence of the digital control lines was significantly reduced by a modified readout sequence of the chip. Before the digital control lines for the readout of the chip are activated, the analog supply voltages of the discriminators are turned off so that the switching noise does not cause noise events in the counters any more. As a result, the chip could be operated with a threshold of about $1300 e^-$. This is demonstrated by a flat field image of a Si sensor taken with 6 keV photons of ^{55}Fe shown in Fig. 9 (6 keV energy deposition corresponds to approximately 1600 electron-hole pairs in Si).

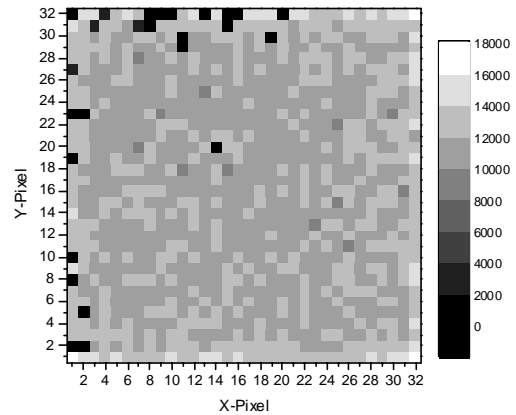


Fig. 9. Flat field image of a Si sensor taken with 6 keV photons of ^{55}Fe (adjusted threshold set to $1300 e^-$).

It can be seen that the bump yield close to the upper and the left edge of the chip is not very good while all other areas of the chip show a good bump yield. Fig. 10 shows an example of a radiograph of a low absorption object. Here a mosquito was exposed to 6 keV photons of ^{55}Fe .

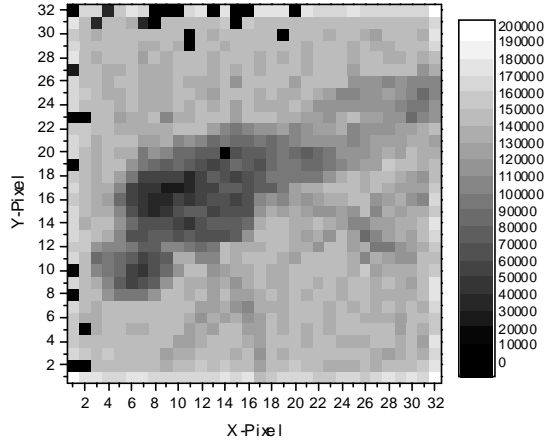


Fig. 10. Radiograph of a mosquito taken with 6 keV photons of ^{55}Fe (Si sensor, adjusted threshold set to 1300 e^-).

A flat field image taken with a CdTe sensor is depicted in Fig. 11. Only 4 pixels out of 1024 are not connected to the sensor, which proves an excellent bump yield achieved with gold stud bump bonding. However, in the flat field image a column pattern of the count rate distribution is visible. As the CdTe sensor is symmetric row- and column-wise, this phenomenon must be induced by the readout chip in combination with the gold studs arrangement, which, indeed, has a column dependence. The origin of this non-uniform behavior is still under investigation. Nevertheless, the detector is fully functional, which is demonstrated in Fig. 12 by a radiograph of a screw nut taken with 60 keV photons of ^{241}Am . The use of 6 keV photons of ^{55}Fe for imaging purposes is not possible since the necessary threshold of about 1100 e^- can not be achieved with our CdTe detector (6 keV energy deposition corresponds to approximately 1300 electron-hole pairs in CdTe).

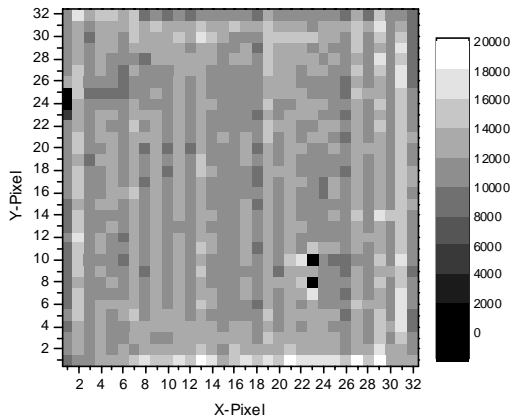


Fig. 11. Flat field image of a CdTe sensor taken with 60 keV photons of ^{241}Am (without threshold adjustment).

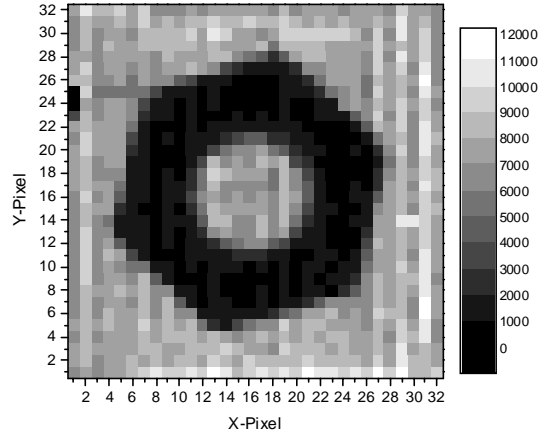


Fig. 12. Radiograph of a screw nut taken with 60 keV photons of ^{241}Am and CdTe sensor (without threshold adjustment).

IV. MEASUREMENTS WITH MULTI CHIP MODULES

A. Si sensor MCM and CdTe sensor MCM

Available bump bonding techniques for MCM construction are wafer-level processes based on In or PbSn bumps, and with these methods Si sensor MCMs for high energy physics experiments have been successfully built [23], [25]-[27]. For the Si sensor MCM described in this work a PbSn bump bonding process was used, which is not optimal for single dies. Each chip has to be inserted in a dummy wafer, in which an exactly machined opening was cut before. After PbSn bump balls are deposited on the chip by a planar process, the chip is removed out of the dummy wafer again, cleaned along the edges and then can be used for flip chip bump bonding to the Si sensor. The risk of bump damage near the chip edges is high. In Fig. 13 a flat field image taken with a Si sensor MCM is presented, and defect pixels exist mainly along the chip edges. The overall bump yield is 91.8 %. In Fig. 13 it also can be seen that pixels along the symmetry axes of the MCM have a higher count rate due to the larger area of the corresponding sensor pixels (cf. Fig. 2). The image was taken without threshold adjustment because a shift register which is necessary for the fine adjustment was damaged during module assembly.

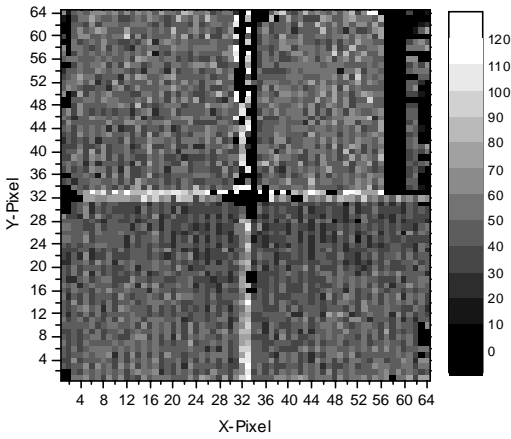


Fig. 13. Flat field image of a Si sensor MCM taken with 60 keV photons of ^{241}Am (without threshold adjustment).

For future biomedical applications, the challenge is to build MCMs with large area CdTe sensors. In contrast to the above mentioned techniques, the CdTe sensor MCM is bump bonded by a gold stud process. This process does not require a full wafer but can be done with single chip dies. A flat field image taken with a CdTe MCM is shown in Fig. 14.

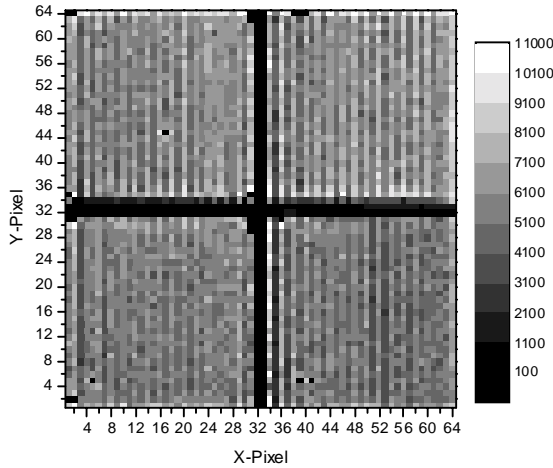


Fig. 14. Flat field image of a CdTe sensor MCM taken with 60 keV photons of ^{241}Am (without threshold adjustment).

It can be seen that along the two axes of the module many defective pixels occur. These have either a completely vanishing or a very low count rate. A possible explanation are fractures of the detector along the two axes. The detector regions close to the fractures would not work any more or would have a very low charge collection efficiency. This could account for the gradations in pixel count rates near the axes. A fracture of the CdTe is not unlikely because the very fragile 0.5 mm thick sensor is mechanically stressed during bump bonding to the readout chips and during wire bonding to the hybrid

PCB. It should be stated that all other regions of the MCM show a very good bump yield. When pixels at the symmetry axes of the module are not taken into account, the bump yield for the whole MCM is 99 %. Indeed, the column pattern in the count rate distribution of Fig. 14 is similar to that of the single chip CdTe detector (Fig. 11), which implies a similar quality of bump bonding. An example of the imaging performance of the CdTe sensor MCM is presented in Fig. 15, which shows a radiograph of a cogwheel.

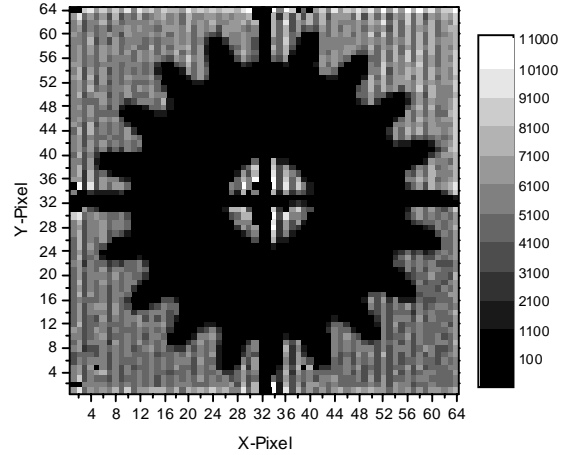


Fig. 15. Radiograph of a cogwheel taken with 60 keV photons of ^{241}Am and CdTe sensor MCM (without threshold adjustment).

V. SUMMARY

The MPEC 2.3 chip was successfully characterized as a low noise, single photon counting readout chip for pixel detectors. By dynamically adjusting the thresholds a very low threshold dispersion could be achieved. A single chip Si detector of 300 μm thickness and a single chip CdTe detector of 500 μm thickness were assembled and operated. In addition a Si sensor MCM and, for the first time, a photon counting MCM with a CdTe sensor were built. Two bonding techniques were used; solder bump bonding for the Si sensors and gold stud bump bonding for the CdTe sensors.

The solder bump bonding is a wafer-level based process for which the single diced MPEC chips have to be inserted into dummy wafers. Gold stud bump bonding showed a very good bump yield, especially in the case of a single chip detector. It should be noted that imaging performance was affected by a column-dependent count rate distribution. The origin of this effect is unknown. As for assembly of the CdTe sensor MCM, special care must be taken when applying mechanical forces to avoid fracturing the thin sensor.

All measurements were performed with a newly developed USB based readout system. Its compact size and self-powering capability make the whole system easy to use and versatile for different applications.

VI. ACKNOWLEDGMENT

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